This listing of claims will replace all prior versions, and listings, of claims in the application:

The Status of the Claims

1. (Currently Amended) A method for making shallow trench type pixel for complimentary metal oxide semiconductor (CMOS) image sensor, comprising:

forming a CMOS image sensor on an epitaxial wafer having a structure including an epitaxial layer doped with a low concentration positioned on a p-type or n-type substrate doped with a high concentration;

forming a first photoresist layer over said structure, patterning the photoresist layer, and etching the epitaxial layer so as to form a shallow trench on a pixel area~~, and, etching~~;

removing said first photoresist layer;

forming a second photoresist layer over said structure, ~~pattering~~ patterning so as to form a photodiode junction in at least a portion of the shallow trench of the pixel area, and, then, conducting ion-implanting process; and

removing said second photoresist layer and conducting a thermal treatment process.

2. (Original) A method as defined by claim 1, wherein said first and second photoresist layers are removed by an ashing process.

3. (Original) A method as defined by claim 1, wherein said thermal treatment is performed by rapid thermal annealing (RTA) or furnace annealing in the temperature range of 50~400 degree Centigrade.

4. (Original) A method as defined by claim 1, wherein a final profile doped in said epitaxial layer doped with a low concentration is formed on the top of a shallow trench isolation layer.

5. (Original) A method as defined by claim 1, wherein the shallow trench has a depth of 10~10000 angstroms.

6. (Original) A method as defined by claim 1, wherein the shallow trench is filled with a dielectric selected from the group consisting of oxide, nitride, oxinitride, and silicate glass by spin coating, chemical vapor deposition (CVD), or diffusion methods.